

AMENDMENTS TO THE CLAIMS

1. (currently amended) An imaging device comprising:

a plurality of active pixel sensor cells, each having a photosensor, a row select transistor, and an output transistor including a gate connected to a pixel output signal voltage; and

a readout circuit connectable to each of said ~~APS~~ active pixel sensor cells, said readout circuit including an amplifier, said amplifier comprising a first branch including the row select transistor and the output transistor of each of a plurality of said active pixel sensor cells and a first transistor having a different conductivity type than a conductivity type of the row select and output transistors, said amplifier comprising a second branch including at least a second transistor having a same conductivity type as the first transistor, a source follower transistor and at least one additional transistor having a same conductivity type as the row select and output transistors.

2. (original) The imaging device of claim 1, wherein the amplifier provides a gain of about one or higher.

3. (currently amended) ~~The imaging device of claim 1,~~ An imaging device comprising:

a plurality of active pixel sensor cells, each having a photosensor, a row select transistor, and an output transistor including a gate connected to a pixel output signal; and

a readout circuit connectable to each of said active pixel sensor cells, said readout circuit including an amplifier, said amplifier including the row select transistor

and the output transistor of each of a plurality of said active pixel sensor cells, wherein the amplifier comprises:

a first branch comprising:

a first transistor having a drain connected to a first voltage source;

the row select transistor of each pixel; and

the output transistor of each pixel;

a second branch comprising:

a second transistor having a drain connected to the first voltage source;

a third transistor having a gate connected to a second voltage source; and

a source follower transistor having a drain connected to a source of each of the third transistor and the output transistor of each pixel.

4. (original) The imaging device of claim 3, wherein the first voltage source comprises V_{DD} .

5. (original) The imaging device of claim 3, wherein each of the first and second transistors comprise a p-type transistor and each of the row select transistors, output transistors, third transistor, and source follower transistor comprise an n-type transistor.

6. (original) The imaging device of claim 3, further comprising a fourth transistor connected between the third transistor and the source follower transistor, said fourth transistor comprising a gate connected to the first voltage source.

7. (original) The imaging device of claim 3, wherein each pixel and the amplifier are connected to a column line, and further comprising a switch in each pixel to shield the output transistor from voltage changes in the column line.

8. (original) The imaging device of claim 7, wherein the switch comprises a blocking transistor connected between a drain of the output transistor and the first transistor, said blocking transistor having a gate connected to a gate of the row select transistor.

9. (currently amended) The imaging device of claim ~~[[1]]~~ 3, further comprising a gain selector to enable a change in gain in the amplifier.

10. (original) The imaging device of claim 3, further comprising a gain selector to enable a change in gain in the amplifier, said gain selector comprising:

a first gain transistor having a drain connected to the first voltage source; and

a first gain-enable transistor connected between a source of the gain transistor and the source of the first transistor,

wherein while the first gain-enable transistor is conducting, the first transistor and the first gain transistor are connected in parallel.

11. (original) The imaging device of claim 10, wherein the gain selector further comprises:

a second gain transistor having a drain connected to the first voltage source;
and

a second gain-enable transistor connected between a source of the second gain transistor and the source of the second transistor,

wherein while the second gain-enable transistor is conducting, the second transistor and the second gain transistor are connected in parallel.

12. (original) The imaging device of claim 10, wherein each of the first gain transistor and the first gain enable transistor is p-type transistor.

13. (currently amended) An imaging device comprising:

a plurality of active pixel sensor cells, each having a photosensor, a row select transistor, and an output transistor including a gate connected to a pixel output signal ~~voltage~~; and

a readout circuit connectable to each of said APS active pixel sensor cells, said readout circuit including an amplifier, said amplifier comprising:

a first branch comprising:

a first transistor having a drain connected to a first voltage source;

the row select transistor of each pixel; and

the output transistor of each pixel;

a second branch comprising:

a second transistor having a drain connected to the first voltage source;

a third transistor having a gate connected to a second voltage source;

a fourth transistor; and

a source follower transistor having a drain connected to a source of each of the fourth transistor and the output transistor of each pixel.

14. (original) The imaging device of claim 13, wherein the amplifier provides a gain of about one or higher.

15. (currently amended) The imaging device of claim 13, wherein the first voltage source comprises V_{DD} .

16. (original) The imaging device of claim 13, wherein each of said transistors comprise a MOSFET.

17. (currently amended) The imaging device of claim 13, wherein each of the first and second transistors comprise a p-type transistor and each of the row select transistors, output transistors, third transistor, fourth transistor, and source follower transistor comprise an n-type transistor.

18. (new) The imaging device of claim 13, further comprising a gain selector to enable a change in gain in the amplifier.

19. (new) A differential amplifier for reading a pixel output signal, said amplifier comprising:

a first branch comprising:

a first transistor having a drain connected to a first voltage source,

a row select transistor of a pixel, and

an output transistor of the pixel; and

a second branch comprising:

a second transistor having a terminal connected to the first voltage source,

a third transistor having a gate connected to a second voltage source,

a fourth transistor, and

a source follower transistor having a terminal connected to a terminal of the fourth transistor and the output transistor of the pixel.

20. (new) The differential amplifier of claim 19, wherein the amplifier provides a gain of about one or higher.

21. (new) The differential amplifier of claim 19, wherein the first voltage source comprises a power supply voltage.

22. (new) The differential amplifier of claim 19, wherein each of said transistors comprise a MOSFET.

23. (new) The differential amplifier of claim 19, wherein each of the first and second transistors comprise a p-type transistor and each of the row select transistor, output transistor, third transistor, fourth transistor, and source follower transistor comprise an n-type transistor.

24. (new) A differential amplifier for reading a pixel output signal, said amplifier comprising:

a first branch comprising:

a first transistor having a terminal connected to a first voltage source,

a row select transistor of a pixel, and

an output transistor of the pixel; and

a second branch comprising:

a second transistor having a terminal connected to the first voltage source,

a third transistor having a gate connected to a second voltage source, and

a source follower transistor having a drain connected to a source of each of the third transistor and the output transistor of the pixel.

25. (new) The differential amplifier of claim 24, wherein the amplifier provides a gain of about one or higher.

26. (new) The differential amplifier of claim 24, wherein each of the first and second transistors comprise a p-type transistor and each of the row select transistor, output transistor, third transistor, fourth transistor, and source follower transistor comprise an n-type transistor.